1 - 15. (Cancelled)

16.   (Currently amended) A system for packet classification, comprising:

a pre-processor configured to:

        assign an associated identifier to a field within a header of an incoming

packet; and

        store the associated identifier within a header array;

a first memory device including a first set of binary patterns;

a second memory device including a second set of binary patterns;

a third memory device having ~~including~~ instructions ~~configured~~ stored thereon to

process the first set of binary patterns and the second set of binary patterns; and

        a processor configured to match the associated identifier with one or more

patterns from either the first set of binary patterns or the second set of binary patterns

using a range of values associated with each of the first set of binary patterns and the

second set of binary patterns and to process the one or more patterns in accordance a

priority computation to determine which one of the instructions is to be used to process

the incoming packet.

17.   (Original) The system of claim 16, wherein the field is a network address.

18.   (Previously Presented) The system of claim 16, further comprising:

a fourth memory device configured to store a result corresponding to the matched

pattern received from the processor.

19.   (Previously Presented) The system of claim 16, further comprising:

means for determining priority among the one or more patterns.

20.   (Currently amended) A method for packet classification, comprising:

assigning an associated identifier to a field within a header of an incoming packet;

storing the associated identifier within a header array;

maintaining a first set of binary patterns in a first memory device and a second set of binary patterns in a second memory device;

matching the associated identifier with one or more patterns from either the first set of binary patterns or the second set of binary patterns using a range of values associated with each of the first set of binary patterns and the second set of binary patterns; and

processing the one or more patterns in accordance a priority computation to determine which one of the instructions is to be used to process the incoming packet.

21.   (Previously Presented)   An apparatus for packet classification, comprising:

a processor array containing a plurality of processing elements, wherein each processing element is configured to: (i) compare a classification record derived from an incoming packet with one or more patterns associated with rules to be enforced by performing programmed relational operations, and (ii) capture state information in a shift register that is shared by more than one of the processing elements;

an instruction decoder configured to suspend operations for a set of the processing elements and to restart operations for the set of processing elements;

at least one priority encoder configured to determine a highest priority from the state information from the shift registers; and

a record memory configured to be addressed for read and write capabilities, wherein writes are executed to indicate which of several simultaneously processed packets is being submitted to the apparatus for packet classification, and wherein reads are executed to indicate which bit or bits are to be provided to the processor array from all of the simultaneously processed packets.

22.   (Previously Presented)   The apparatus of claim 21, wherein the programmed relational operations include at least one of a group consisting of: an equality operation, less than or equal to operations, and greater than or equal to operations.

23.   (Previously Presented) The apparatus of claim 21, further comprising:

an instruction memory containing instructions configured to: (i) select which bit or bits of the simultaneously processed packets are to be examined by the processor array, and (ii) determine how the selected bit or bits are to be compared against one or more of the patterns.

24.   (Previously Presented)   The apparatus of claim 23, wherein the instructions in the instruction memory are a classification program, wherein the classification program contains further instructions to divide the classification program

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into subsets of sequential instructions, each of which represents a subset of rules defined by the classification program.

25.   (Previously Presented) The apparatus of claim 24, wherein a prioritized relationship exists between a pair of the subsets of the rules defined by the classification program.

26.   (Previously Presented) The apparatus of claim 24, wherein the record memory is configurable to be rewritable during execution of the classification program such that a result from the priority encoder is subsequently examined by the classification program.

27.   (Previously Presented) The apparatus of claim 26, wherein the result includes a current highest priority match as determined by the priority encoder.

28.   (Previously Presented) The apparatus of claim 24, wherein one or more bits selected from one of the classification records in the record memory determine a subset of instructions in the classification program to apply to one or more of the classification records.

29.   (Original) The apparatus of claim 28, wherein the one or more bits selected are selected under programmed control.

30.   (Previously Presented) The apparatus of claim 28, further comprising:

a first memory device configured to store a first subset of the one or more patterns; and

a second memory device configured to store a second subset of the one or more patterns, wherein the classification program retrieves the first subset of the one or more patterns while the second subset of the one or more patterns is being updated.

31.   (Previously Presented) The apparatus of claim 28, further comprising: means for increasing an effective size of the classification program.

32.   (Previously Presented) The apparatus of claim 28, further comprising: means for scaling a number of processing elements applied to a single incoming packet.

33.   (Previously Presented) The apparatus of claim 28, further comprising: means for scaling a number of simultaneously processed packets.

34.   (Previously Presented) The apparatus of claim 28, further comprising: means for scaling a number of packet bits used to select a classification program.

35.   (Original) The apparatus of claim 28, wherein multiple instances of the apparatus are cascaded such that a first instance of the apparatus feeds into a second instance of the apparatus.

36.   (Original) The apparatus of claim 21, wherein multiple instances of the apparatus are cascaded such that a first instance of the apparatus feeds into a second instance of the apparatus.

37.   (New) The system of claim 16, wherein the header array is stored within the header of the incoming packet.

38.   (New) The method of claim 20, further comprising:

selecting, prior to the assigning, the associated identifier from either the first set of binary patterns or the second set of binary patterns; and

wherein the matching further comprises:

matching the associated identifier with one or more patterns from a selected one of the first set of binary patterns or the second set of binary patterns; and

allowing the non-selected one of the first set of binary patterns or the second set of binary patterns to be updated during the matching.